

SK hynix e-NAND Product Family **eMMC5.1 Compatible**

Revision History

Revision No.	History	Date	Remark
1.0	- 1 st Official release	Aug. 31, 2015	

Table of Contents

1. Introduction	4
1.1 General Description	4
1.2 Product Line-up	4
1.3 Key Features	4
2. Package Configurations	5
2.1 Pin connection	5
2.2 Package Mechanical Drawing	7
3. e-NAND Characteristics	8
3.1 Performance	8
3.2 Power	9
4. e-NAND new features (eMMC5.0 and eMMC5.1).....	10
4.1 eMMC5.0 New features.....	10
4.1.1 HS400 mode	10
4.1.2 Field firmware update	17
4.1.3 Health(Smart) report	20
4.1.4 Production state awareness	21
4.1.5 Sleep notification	23
4.1.6 Secure removal type	24
4.2 eMMC5.1 New features.....	25
4.2.1 Command queuing	25
4.2.2 Cache barrier	26
4.2.3 Cache Flushing report	28
4.2.4 Background operation(BKOP) control	28
4.2.5 Secure Write Protection	29
4.2.6 Enhanced strobe	34
4.2.7 RPMB throughput improvement	38
5. e-NAND general parameters	39
5.1 Timing	39
5.2 Bus signal	44
5.3 Power mode	48
5.4 Connection guide	52
6. e-NAND basic operations	53
6.1 Partitioning	53
6.2 Boot operation	56
7. Timeout	57
8. Register	58
8.1 Operation conditions register (OCR)	58
8.2 Card identification (CID) register	59
8.3 Card specific data register(CSD)	59
8.4 Extended CSD register	62
8.5 RCA (Relative Card Address)	68
8.6 DSR (Driver Stage Register)	68

1. Introduction

1.1 General Description

SK hynix e-NAND consists of NAND flash and MMC controller.

e-NAND has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. e-NAND protects the data contents from the host sudden power off failure.

e-NAND is compatible with JEDEC standard eMMC5.1 specification. (Except CMD queue)

1.2 Product Line-up

Density	Part Number	NAND Stack	PKG Size (mm)	Package Type
8GB	H26M41204HPR	64Gb x 1	11.5x13x0.8	153FBGA

1.3 Key Features

- **eMMC5.1 compatible**

(Backward compatible to eMMC4.5 & eMMC5.0)

- **Bus mode**

- Data bus width : 1bit(default), 4bits, 8bits
- Data transfer rate: up to 400MB/s (HS400)
- MMC I/F Clock frequency : 0~200MHz
- MMC I/F Boot frequency : 0~52MHz

- **Operating Voltage Range**

- V_{CC} (NAND) : 2.7V - 3.6V
- V_{CCQ} (Controller) : 1.7V - 1.95V / 2.7V ~ 3.3V

- **Temperature**

- Operation (-25°C ~ +85°C)
- Storage without operation (-40°C ~ +85°C)

- **Others**

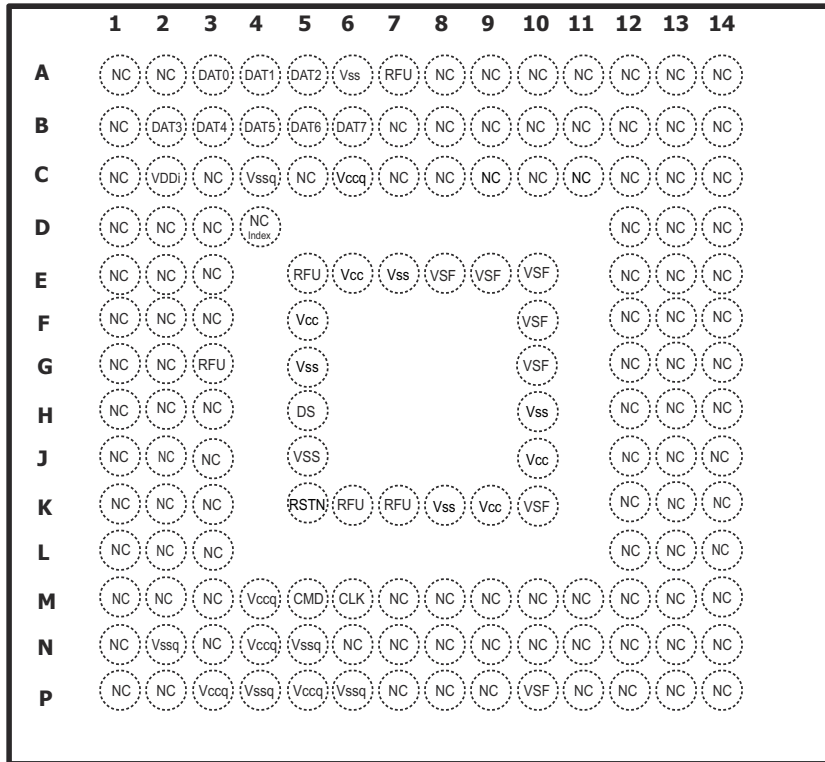
- This product is compliance with the RoHS directive

- **Supported Features**

- HS400, HS200
- HPI, BKOPS, **BKOP operation control**
- Packed CMD
- Cache, **Cache barrier, Cache flushing report**
- Partitioning, RPMB, RPMB throughput improve
- Discard, Trim, Erase, Sanitize
- Write protect, Secure write protection
- Lock/Unlock
- PON, Sleep/Awake
- Reliable Write
- Boot feature, Boot partition
- HW/SW Reset
- Field Firmware Update
- Configurable driver strength
- Health(Smart) report
- Production state awareness
- Secure removal type
- Data Strobe pin, **Enhanced data strobe**
(Bold features are added in eMMC5.1)

2. Package Configurations

2.1 Pin connection



[Figure 1] FBGA153 Package Connection (Top view through Package)

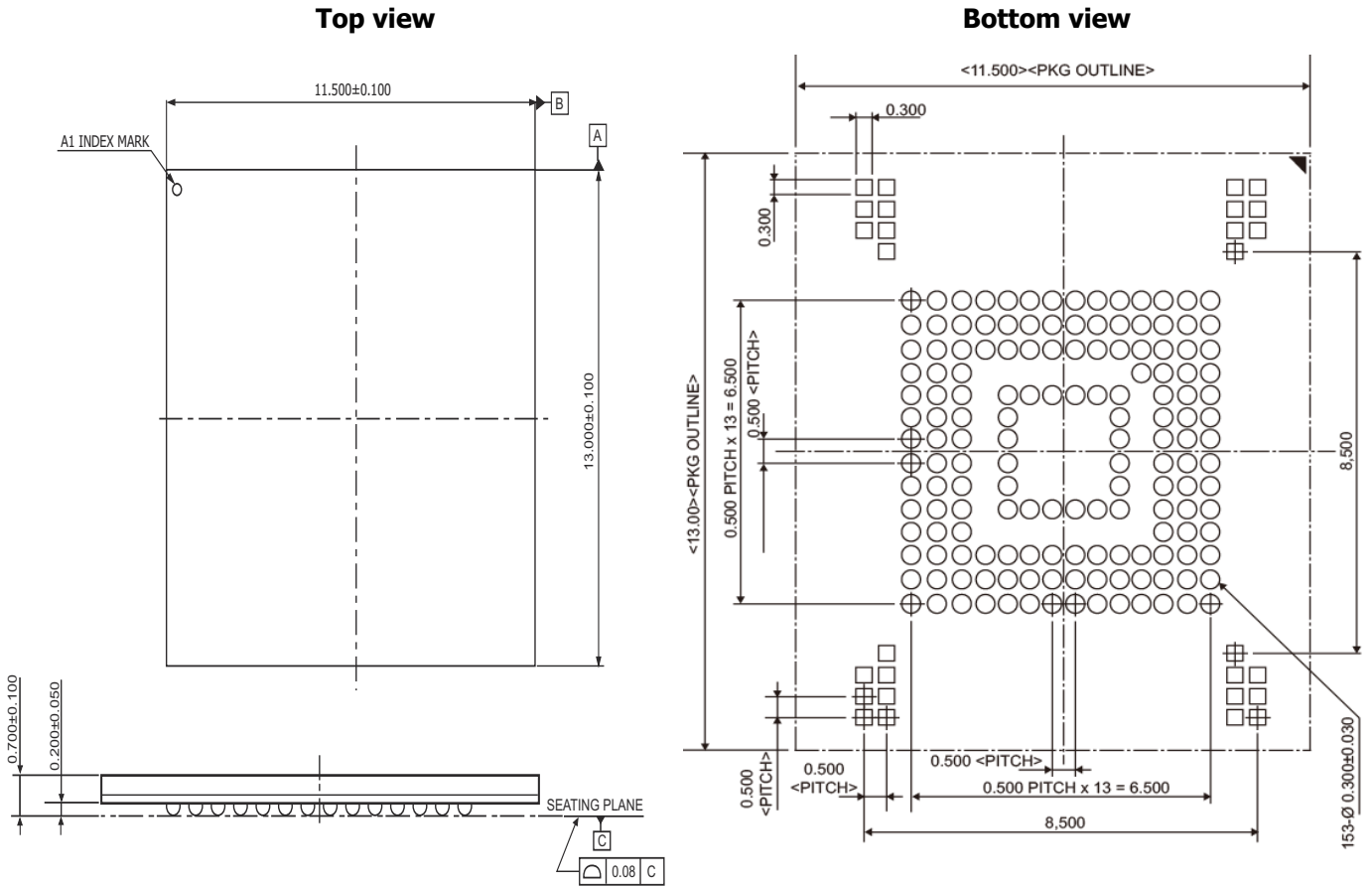
Pin number	Name	Pin number	Name	Pin number	Name	Pin number	Name
A3	DAT0	C4	V _{ssq}	G10	VSF	M5	CMD
A4	DAT1	C6	V _{ccq}	H5	DS	M6	CLK
A5	DAT2	E6	V _{cc}	H10	V _{ss}	N2	V _{ssq}
A6	V _{ss}	E7	V _{ss}	J5	V _{ss}	N4	V _{ccq}
B2	DAT3	E8	VSF	J10	V _{cc}	N5	V _{ssq}
B3	DAT4	E9	VSF	K5	RSTN	P3	V _{ccq}
B4	DAT5	E10	VSF	K8	V _{ss}	P4	V _{ssq}
B5	DAT6	F5	V _{cc}	K9	V _{cc}	P5	V _{ccq}
B6	DAT7	F10	VSF	K10	VSF	P6	V _{ssq}
C2	VDDi	G5	V _{ss}	M4	V _{ccq}	P10	VSF

Name	Type	Ball No.	Description
CLK	Input	M6	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.
CMD	Input	M5	Command: A bidirectional channel used for device initialization and command transfers. Command has two operating modes: 1) Open-drain for initialization. 2) Push-pull for fast command transfer.
DAT0	I/O	A3	Data I/O0: Bidirectional channel used for data transfer.
DAT1	I/O	A4	Data I/O1: Bidirectional channel used for data transfer.
DAT2	I/O	A5	Data I/O2: Bidirectional channel used for data transfer.
DAT3	I/O	B2	Data I/O3: Bidirectional channel used for data transfer.
DAT4	I/O	B3	Data I/O4: Bidirectional channel used for data transfer.
DAT5	I/O	B4	Data I/O5: Bidirectional channel used for data transfer.
DAT6	I/O	B5	Data I/O6: Bidirectional channel used for data transfer.
DAT7	I/O	B6	Data I/O7: Bidirectional channel used for data transfer.
RSTN	Input	K5	Reset signal pin
V _{cc}	Supply	E6,F5,J10,K9	V _{cc} : Flash memory I/F and Flash memory power supply.
V _{ccq}	Supply	C6,M4,N4,P3,P5	V _{ccq} : Memory controller core and MMC interface I/O power supply.
V _{ss}	Supply	A6,E7,G5,H10,J5,K8	V _{ss} : Flash memory I/F and Flash memory ground connection.
V _{ssq}	Supply	C4,N2,N5,P4,P6	V _{ssq} : Memory controller core and MMC I/F ground connection
VDDi		C2	VDDi: Connect 0.1uF capacitor from VDDi to ground.
DS	Out put	H5	DS: Data Strobe
VSF	Supply	E8,E9,E10,F10, G10, K10, P10	VSF: Vendor Specific Function SK hynix use E9, E10 Pin as VSF Pin
RFU			Reserved for future use

[Table 1] FBGA153 Ball Description

2.2 Package Mechanical Drawing

2.2.1 11.5mm x13.0mm x0.8mm



[Figure 2] 11.5mm x 13.0mm x 0.8mm Package dimension

SK hynix



H26M41204HPR

e-NAND 626A

• H3BVC356R04