2N7002K

List

2N7002K

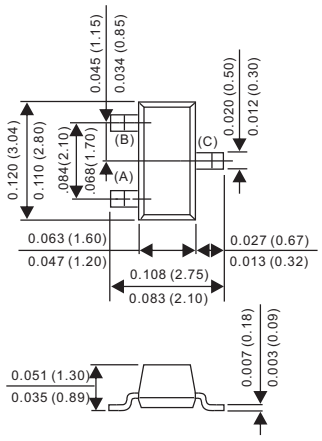
60V N-Channel Enhancement Mode MOSFET- ESD Protection

Features

- $R_{DS(ON)}$, V_{GS}@10V, I_D@500mA=3.0 Ω
- $R_{DS(ON)}$, V_{GS}@4.5V, I_D@200mA=4.0 Ω
- ESD protection 2KV (Human body mode)
- Advanced trench process technology.
- High density cell design for ultra low on-resistance.
- Very low leakage current in off condition
- Specially designed for battery operated system, solid-state relays drivers, relays, displays, lamps, solenoids, memories, etc.
- In compliance with EU RoHS 2002/95/EC directives.
- Suffix "-H" indicates Halogen-free part, ex. 2N7002K-H.

Package outline

SOT-23



Dimensions in inches and (millimeters)

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Maximum ratings (AT T_A=25°C unless otherwise noted)

PARAMETER	Symbol	Ratings	UNIT
Drain-Source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	±20	V
Continuous drain current	I_D	300	mA
Pulsed drain current [1]	I_{DM}	2000	mA

PARAMETER		Symbol	MIN.	TYP.	MAX.	UNIT
Total power dissipation	P_D@T_A= 25°C P_D@ T_A=75°C	P_D			0.35 0.21	W
Operation junction and storage temperature range		T_J, T_{STG}	-55		+150	°C
Thermal resistance(PCB mounted) [2]	Junction to ambient	$R_{\theta JA}$		357		°C/W

Note : 1. Maximum DC current limited by package

2. Surface mounted on FR4 board, t ≤ 5 sec

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Electrical characteristics (AT T_A=25°C unless otherwise noted)

STATIC

PARAMETER	CONDITIONS	Symbol	MIN.	TYP.	MAX.	UNIT
Drain-source Breakdown Voltage	V_{GS} = 0V, I_D = 10μA	BV_{DSS}	60			V
Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 250μA	$V_{GS(th)}$	1.0		2.5	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 500mA	$R_{DS(on)}$			3.0	Ω
	V_{GS} = 4.5V, I_D = 200mA				4.0	
Zero Gate Voltage Drai n Current	V_{DS} = 60V, V_{GS} = 0V	I_{DSS}			1	μA
Gate-Body leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}			±10	μA
Forward TransConductance	V_{DS} = 15V, I_D = 250mA	g_{fs}	100			ms

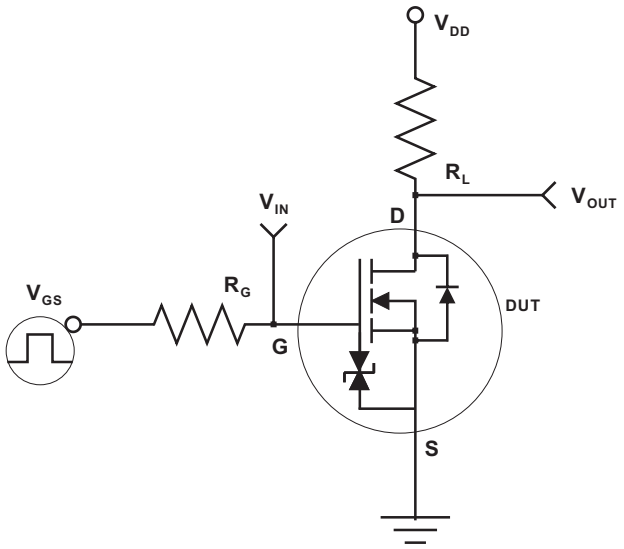
DYNAMIC

Total Gate Charge	V_{DS} = 15V, I_D = 200mA V_{GS} = 4.5V	Q_g			0.8	nC
Turn-On Delay Time	V_{DD} = 30V, R_L = 150Ω, I_D = 200mA, V_{gen} = 10V, R_G = 10Ω	t_{on}			20	ns
Turn-Off Delay Time		t_{off}			40	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V f = 1.0 MHz	C_{iss}			35	pF
Output Capacitance		C_{oss}			10	
Reverse Transfer Capacitance		C_{rss}			5	

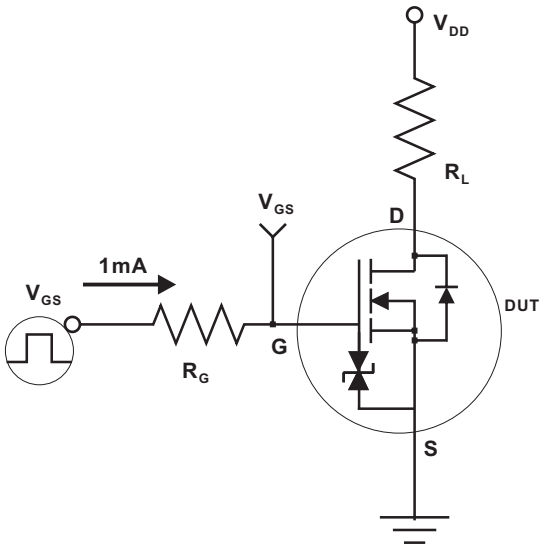
Source-Drain Diode

Diode Forward Voltage	I_S=200mA, V_{GS}=0V	V_{SD}		0.82	1.3	V

Switching Test Circuit



Gate Charge Test Circuit



Rating and characteristic curves (2N7002K)

Fig.1 Output Characteristic

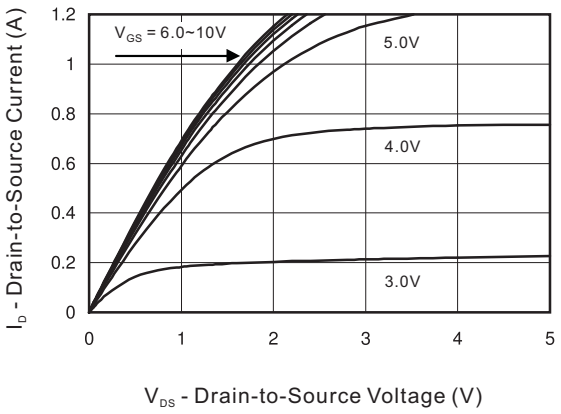


Fig.2 Transfer Characteristic

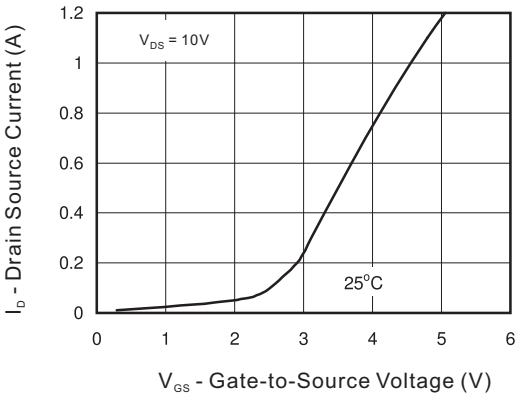


Fig.3 On Resistance vs Drain Current

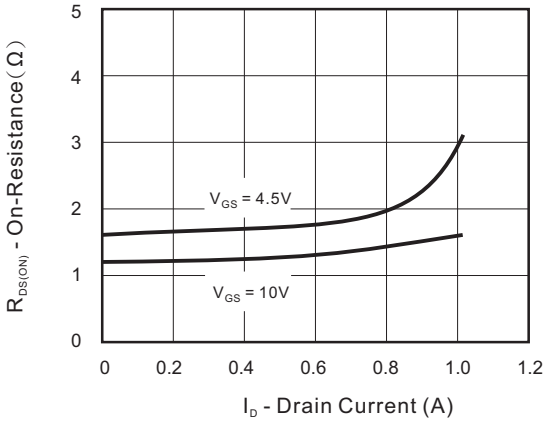


Fig.4 On Resistance vs Gate to Source Voltage

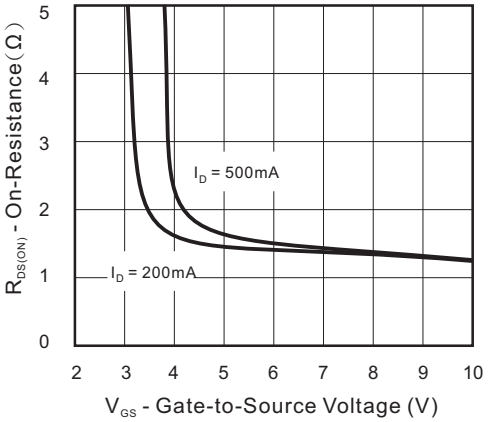
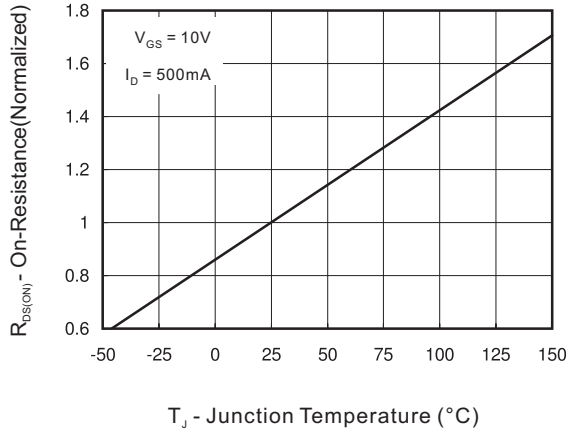


Fig.5 On Resistance vs Junction Temperature



Rating and characteristic curves (2N7002K)

Fig. 6 Gate Charge Waveform

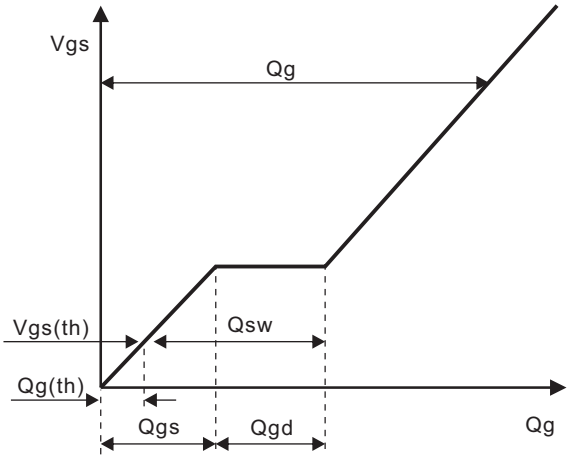


Fig.7 Gate Charge

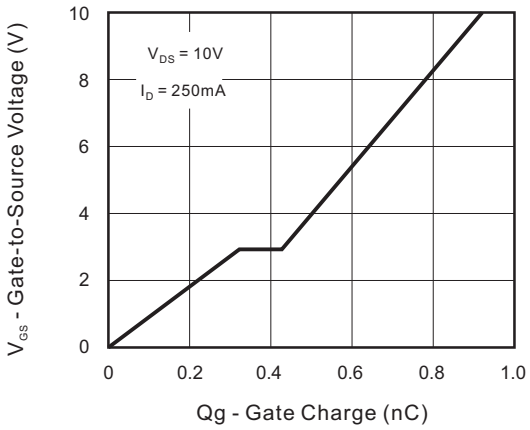


Fig.8 Threshold Voltage vs Temperature

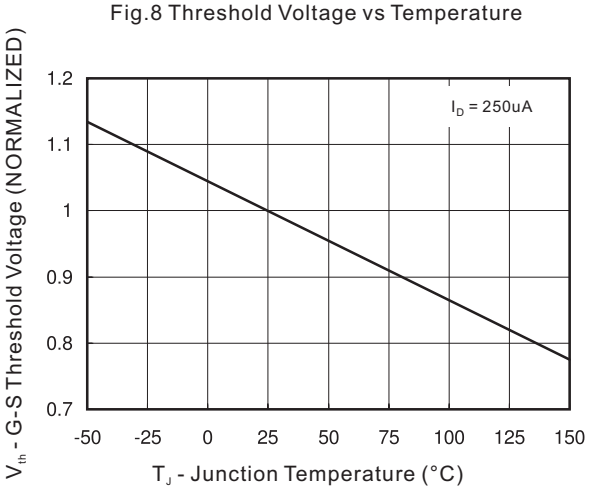


Fig.9 Breakdown Voltage vs Junction Temperature

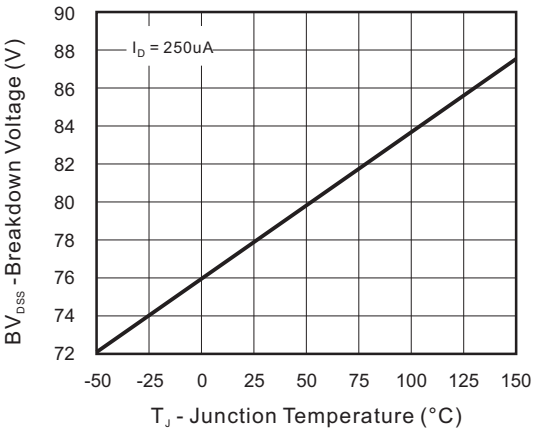
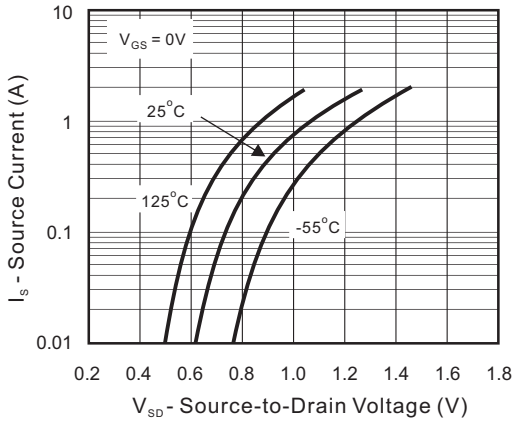


Fig.10 Source-Drain Diode Forward Voltage



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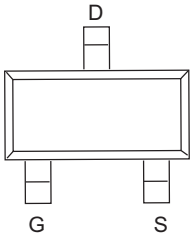
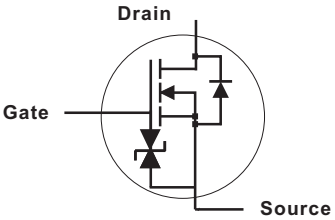
Pinning information

Pin	Simplified outline	Symbol
PinD Drain PinG Gate PinS Source		

Marking

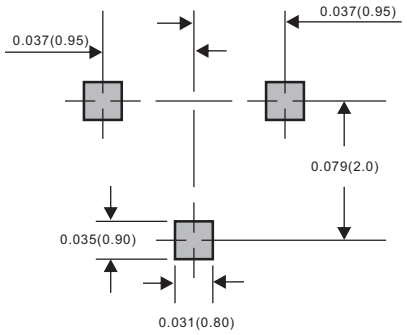
Type number	Marking code	
2N7002K	02K$\overline{\text{YM}}$	(Note 1)
	K72≧	(Note 2)
	RK≧	(Note 2)

Note:1.YM indicate Date ode, ¯ indicate Halogen-Free.
Y= year code, 8=2008, 9=2009
M= week code, A~Z = 1st ~ 26th week
a ~z= 27th ~ 52nd week
. =53rd week
2.M = Month code

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Odd Year	1	2	3	4	5	6	7	8	9	T	V	C
Even Year	E	F	H	J	K	L	N	P	U	X	Y	Z

Suggested solder pad layout

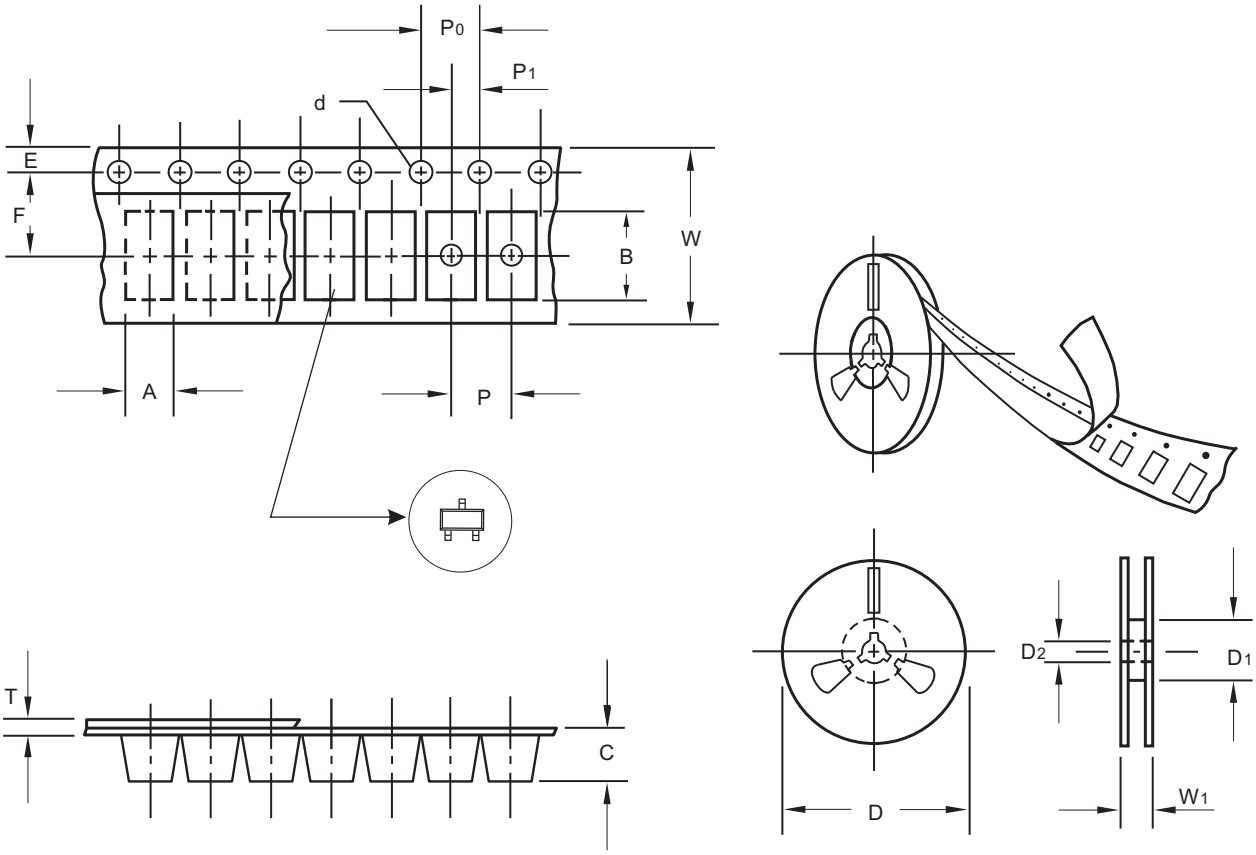
SOT-23



Dimensions in inches and (millimeters)

2N7002K

Packing information



unit:mm

Item	Symbol	Tolerance	SOT-23
Carrier width	A	0.1	3.15
Carrier length	B	0.1	2.77
Carrier depth	C	0.1	1.22
Sprocket hole	d	0.1	1.50
13" Reel outside diameter	D	2.0	-
13" Reel inner diameter	D_1	min	-
7" Reel outside diameter	D	2.0	178.00
7" Reel inner diameter	D_1	min	55.00
Feed hole diameter	D_2	0.5	13.00
Sprocket hole position	E	0.1	1.75
Punch hole position	F	0.1	3.50
Punch hole pitch	P	0.1	4.00
Sprocket hole pitch	P_0	0.1	4.00
Embossment center	P_1	0.1	2.00
Overall tape thickness	T	0.1	0.23
Tape width	W	0.3	8.00
Reel width	W_1	1.0	12.0

Note:Devices are packed in accor dance with EIA standar RS-481-A and specifications listed above.

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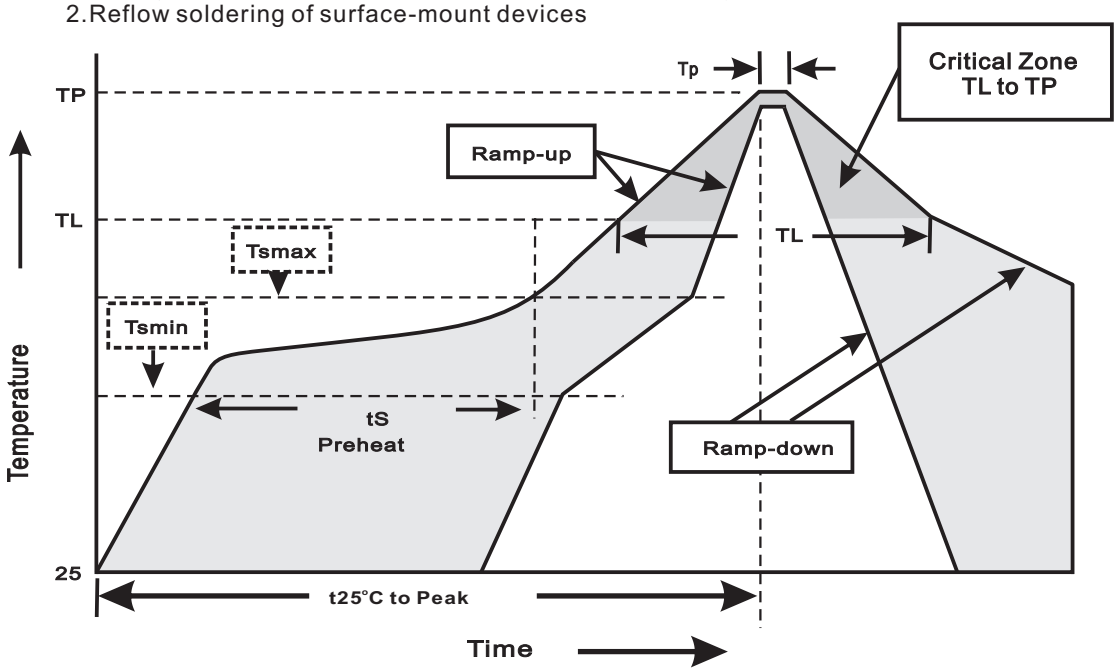
Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA, (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	15,000	183*183*123	178	382*262*387	240,000	11.6

Suggested thermal profiles for soldering processes

1.Storage environment: Temperature=5°C~40°C Humidity=55%±25%
2.Reflow soldering of surface-mount devices



3.Reflow soldering

Profile Feature	Soldering Condition
Average ramp-up rate(T_L to T_P)	<3°C/sec
Preheat -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(min to max)(t_s)	 150°C 200°C 60~120sec
Tsmax to T_L -Ramp-upRate	 <3°C/sec
Time maintained above: -Temperature(T_L) -Time(t_L)	 217°C 60~260sec
Peak Temperature(T_P)	255°C-0/+5°C
Time within 5°C of actual Peak Temperature(t_P)	10~30sec
Ramp-down Rate	<6°C/sec
Time 25°C to Peak Temperature	<6minutes

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High reliability test capabilities

Item Test	Conditions	Reference
1. High Temperature Gate Bias	Ta=150℃ Vgs=0. 8 x BVGSS for 1000hours	JESD22-A108-C
2. High Temperature Reverse Bias	Ta=150℃ Vds=0. 8 x BVDSS for 1000hours	JESD22-A108-C
3. Solder ability Test	Temp=245℃ for 5sec	JESD22-B102-D
4. Pressure Cooker Test	Ta=121℃/100%RH Pressure=2Atm for 168hours	JESD22-A102-C
5. Temperature Cycle Test	-65℃/10min~150℃/10min Transfer<5min. total 1000 cycles.	JESD22-A104-B
6. Temperature Humidity Test	Ta=85℃ Humidity=85%RH for 1000hours	JESD22-A101-B
7. High Temperature Storage Test	Ta=150℃ for 1000hours	JESD22-B103-B